(3 Hours) **[Total Marks: 80]**

N.B: (1) Questions No.1 is compulsory.
(2) Attempt any three questions out of remaining five questions.
(3) Assume suitable data if required.
(4) Figures to the right indicate full marks.

Q.1 Solve any four **20**

a) State the relationship between DTFS, DTFT and DFT.
b) Differentiate FIR and IIR filters.
c) Differentiate fixed point and floating point implementations.
d) A digital filter has the following transfer function. Identify type of filter and justify

$$H(z)=\frac{z}{z+0.5}$$

e) Explain how the speed is improved in calculating DFT by using FFT algorithm.

Q. 2 a) A high pass filter is to be designed with following desired frequency response. **10**

$$H_d(e^{jw}) = 0 \quad -\frac{\pi}{4} \le w \le \frac{\pi}{4}$$
$$= e^{-j2w} \quad \frac{\pi}{4} < |w| \le \pi$$

Determine the filter coefficients h(n) if the window function is defined as

$$w(n) = 1 \quad 0 \le n \le 4$$
$$= 0 \quad \text{otherwise}$$

Also determine the frequency response $H(e^{jw})$ of the designed filter.

b) Compute circular convolution of following sequences using DITFFT and IDITFFT **10**

$x_1(n)=\{1,2,1,2\}$ and $x_2(n)=\{1,2,1\}$

Q 3 a) Explain design steps for to design FIR filter using frequency sampling method. **10**

b) Explain the mapping from S-plane to Z-plane using impulse invariance technique. Also explain the limitations of this method. **10**

Q. 4 a) Design a Chebyshev-I filter with maximum passband attenuation of 2.5 dB at $\Omega p=20$ rad/sec and stopband attenuation of 30dB at $\Omega s=50$ rad/sec. **10**

b) Develop composite radix DIFFFT flow graph for $N=6=3\times2$. **10**

Q. 5 a) Design a digital Butterworth filter that satisfies following constraints using bilinear transformation method. Assume Ts=1s. **10**

$$0.707 \le |H(e^{jw})| \le 1 \quad 0 \le w \le \frac{\pi}{2}$$
$$|H(e^{jw})| \le 0.2 \quad \frac{3\pi}{4} \le w \le \pi$$

b) Explain the effects of finite word length in digital filters with examples. **10**

Q. 6. a) Explain application of DSP processor in ECG signal analysis. **10**

b) Draw neat architecture of TMS320C67XX DSP processor and explain each block. **10**

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