## Paper / Subject Code: 49304 / DIGITAL LOGIC DESIGN AND ANALYSIS

Time: 3 Hours	Marks: 80
N.B. (1) Question No. 1 is compulsory (2)Assume suitable data if necessary (3)Attempt any three questions from remaining questions	
1	
(a) Convert (47.3) <sub>7</sub> to BCD, Excess-3 and gray code.	(3)
(b) Perform (2F9) <sub>H</sub> – (1AD) <sub>H</sub> without converting to any other base.	(3)
(c) Subtract $(64)_{10}$ – $(31)_{10}$ using 2's complement.	(4)
(d) Explain race around condition.	(4)
(e) Prove OR-AND configuration is equivalent to NOR-NOR configu	uration. (4)
(f) Obtain hamming code for data 1101.	(2)
2 (a) Simplify following function using Quine McCluskey method and re using basic gates.	alize circuit (10)
$F(A,B,C,D) = \sum m(0,1,3,5,7,9,11,15) + d(2,14)$	
(b) Design 1-bit magnitude comparator.	(10)
3 (a) Compare different logic families with respect to fan in, fan out, spe	eed, (5)
propogation delay and power dissipation.	(3)
(b) Simplify $Y = \overline{A} \overline{B} \overline{C} + A \overline{B} \overline{C} + A \overline{B} C$	(5)
(c) Implement the following using only one 8:1 Mux and few gates.	(10)
$F(A,B,C,D) = \sum m(0, 1, 5, 7, 9,10,15)$	
	(40)
4 (a) Convert D flip-flop to JK flip-flop and JK flip-flop to D flip-flop.	(10)
(b) Design a full adder using only NAND gates.	(10)
5 (a) Design mod -6 asynchronous UP counter.	(10)
(b) Write short note on VHDL.	(10)
6 (a) Explain Astable and Bistable multivibrators.	(10)
(b) Explain 4-bit bidirectional shift register.	(10)