Con. 5188-09. S.E.(EXTC) Sem III (R) SP-7406

(REVISED COURSE)

Electronic Devices & Circuits-I

(3 Hours) [Total Marks : 100

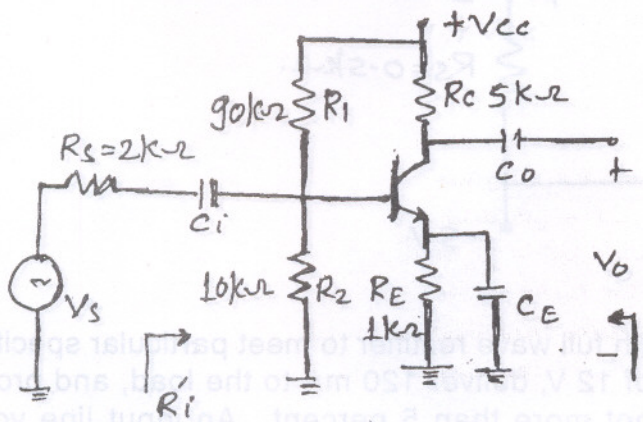
8/12/09
2.30 to 5.30

N.B. : (1) Question No. **1** is **compulsory**.
(2) Out of remaining questions, attempt any **three** questions.
(3) **In all five** questions to be **attempted**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Design single stage RC coupled C E amplifier employing BC 147A to give a voltage gain of $A_V = 100$, $S_{ICO} \leq 10$ and output voltage of $V_0 = 3V$. **15**
   (b) For the above designed amplifier determine; voltage gain, input impedance, output impedance, current supplied by source V_{cc} and voltage gain if capacitor C_e is removed. **5**

2. (a) Design single stage CS amplifier employing JFET type BFW11 with biasing circuit to provide stability of operating Q point against device parameter variation so that $2{\cdot}25\ mA \leq I_D \geq 4{\cdot}2\ mA$ and $A_V = 12$. Use transfer characteristics of JFET from data sheet. Assume $r_d = 50\ k$ for JFET. **15**
   (b) From the design amplifier, determine what will be the maximum output voltage that can be obtained without distortion and corresponding input voltage that can be applied in the worst condition. **5**

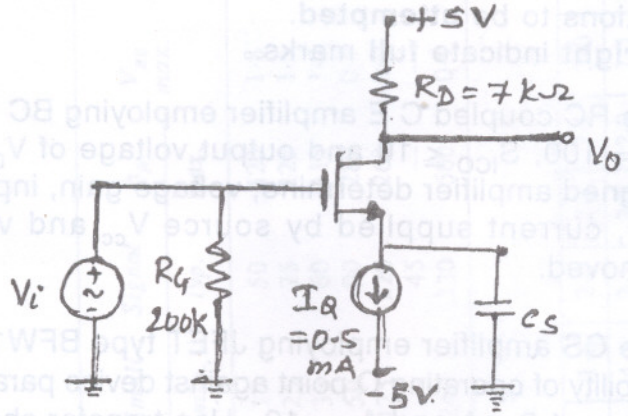
3. (a) Sketch the input output characteristic curves for a transistor in CB connection and show how would obtain the four parameters hib, hfb, hrb, and hob ? Why are h-parameter conversion formulas necessary ? **10**
   (b) The transistor amplifier shown in **figure** has the following parameters : **10**
   $h_{ie} = 2k\Omega$; $h_{fe} = 50$; $h_{re} = 2 \times 10^{-4}$; and $h_{oe} = 20 \times 10^{-6}$ A/V.
   Derive the expression for overall voltage gain A_{vs}, input impedance R_i, and current gain A_{IS} and evaluate the same.



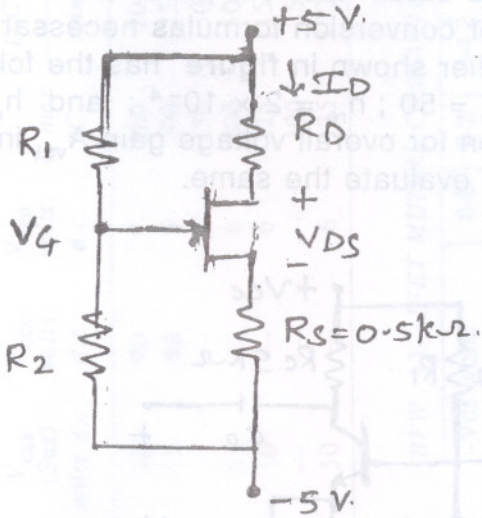
4. (a) In a germanium transistor using potential divider biasing method, the operating point is chosen such that $I_C = 2mA$, $V_{CE} = 4V$. If $R_C = 2\ k\Omega$, V_{CC} 10= V, and $\beta = 50$. Determine the values of R_1, R_2, and R_E. Assume $I_1 = 10\ I_B$. I_1 is current through R_1. **10**
   (b) What is the principle of providing thermal stabilization by means of different methods of transistor biasing ? Explain the bias compensation techniques using a diode and thermistor or sensitor. **10**

[TURN OVER

5. (a) For the circuit shown in **figure** analyze and determine : **10**
   (i) DC bias condition
   (ii) Small-signal voltage gain
   (iii) Input and output impedance.
   V_{TN} = 0·8 V, K_n = 1mA/V^2, and λ = 0·001V^{-1}.

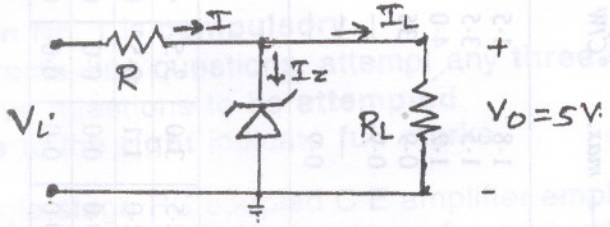


   (b) The parameters of the transistor in the JFET common-source amplifier shown in **figure** are : I_{DSS} = 10 mA, V_p = – 3·5V, $R_1 + R_2$ = 120 kΩ and the Q-point is at I_{DQ} = 5 mA and V_{DS} = 5 V. Determine the values of R_1, R_2 and R_D. **10**



6. (a) Design capacitor filter with full wave rectifier to meet particular specifications. The peak outut voltage of 12 V, deliver 120 mA to the load, and produce an output with a ripple of not more than 5 percent. An input line voltage of 120 V and 50Hz is available. **12**

(b) Design a Zener voltage regulator to meet the following specifications : 8
Output voltage V_0 = 5 V, Load current I_L = 10 mA, Zener wattage = 400 mW and Input voltage V_i = 10 V ± 2V.



7. Write a short notes on following : 20
   (a) UJT relaxation oscillator
   (b) Power MOSFET
   (c) MOSFET biasing
   (d) Critical Inductance in filter.

DBEC DATA SHEET

Transistor type	Pdmax @ 25°C Watts	Icmax @ 25°C Amps	$V_{CE}^{(sat)}$ volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CER} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{BEO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal min.	typ.	h_{fe} max.	V_{BE} max.	θ_{fc} °C/W	Derate above 25°C W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
2CN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4
2CN 149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3
2CN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	0·05
2C147A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	220	260	0·9	—	—
2N. 525(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	—
2C147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—

Transistor type	hie	hoe	hre	θja
2C 147A	2·7 K Ω	18μ ℧	1·5 × 10^{-4}	0·4°C/mw
2N 525 (PNP)	1·4 K Ω	25μ ℧	3·2 × 10^{-4}	—
2C 147B	4·5 K Ω	30μ ℧	2 × 10^{-4}	0·4°C/mw
ECN 100	500 Ω	—	——	——
ECN 149	250 Ω	—	——	——
ECN 055	100 Ω	—	——	——
2N 3055	25 Ω	—	——	——

BFW 11—JFET MUTUAL CHARACTERISTICS

–VGS volts	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
IDS max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·5	0·0
IDS typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
IDS min. mA	4·0	3·0	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel *JFET*

Type	V_{DS} max. Volts	V_{DG} max. Volts	V_{GS} max. Volts	P_d max. @25°C	T_j max.	I_{DSS}	g_{mo} (typical)	$-V_P$ Volts	r_d	Derate above 25°C	θ_{ja}
2N3822	50	50	50	300 mW	175°C	2 mA	3000 μ ℧	6	50 KΩ	2 mW/°C	0·59°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ ℧	2·5	50 KΩ	——	0·59° C/mW