Question Bank. 2

Q.1) With the help of ac equivalent circuit, derive the expressions for input impedence, output impedence & vtg gain for a CS ampl^r with bypassed R_S
(Assume self biasing used)

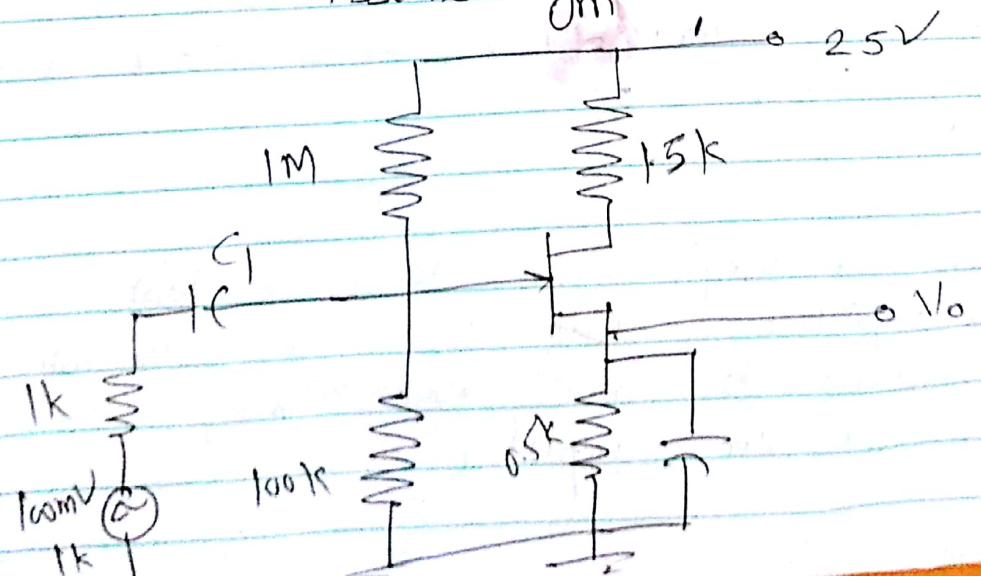
Q.2 Q.1 For vtg divider biasing

Q.3- Z_i, Z_o, A_V For CS configuration voltage divider biasing unbypassed R_S.

Q.4 With the help of ac equivalent ckt, derive the expressions for i/p impe., o/p impe. & vtg gain for the ~~CS FET~~ Source follower configuration.
(Assume self biasing used)

Q.5) For the circuit shown, determine the output vtg V_o & o/p resi.

Assume g_m = 5mA/V & r_d = 10 k



Q.6) Compare CS, CD & CG amplifier with all its parameters.

Q.7) Design an amplifier with CE configuration with the specification,

$h_{fe} = 220$, $h_{ie} = 2.7\ k\Omega$

$h_{oe} = h_{re} = 0$, $S_{ICO} \leq 10$

Ampl^r having,

$|A_V| \geq 180$, $V_{IO} = 3\ V_{olts}$, $V_{CC} = 18V$

$f_L \leq 20\ Hz$

Q.8) Design un-bypassed single stage RC coupled amplifier.

Given,

$V_{CE} = 9V$, $h_{fe} = 100$, $A_V = 10$

$V_{O(p-p)} = 5V$, $R_L = 4.5k$, $f_L = 125\ Hz$

Q.9) Design a C-E amplifier with V_{fg}. divider bias (self bias) that uses silicon transistor with $I_E = 1.53\ mA$, $V_{BE} = 0.6V$, $V_{CE} = 22.5\ V$ & $R_C = 5.6\ k$. It's desired to establish a Q-point at $V_{CE} = 12\ V$, $I_C = 1.5\ mA$ & a stability factor $= 3$.

Q.10) Design a single stage RC coupled CE amplifier using BJT with following specifications to meet the following spec^i of an amplifier.

$h_{fe} = 300$, $h_{ie} = 2.2k\Omega$

$h_{oe}, h_{re} = 0$

$|A_v| \geq 200$, $S_{ICO} \leq 10$, $V_o = 5V_{rms}$

$V_{CE} = 20V$, $f_L = 30Hz$.

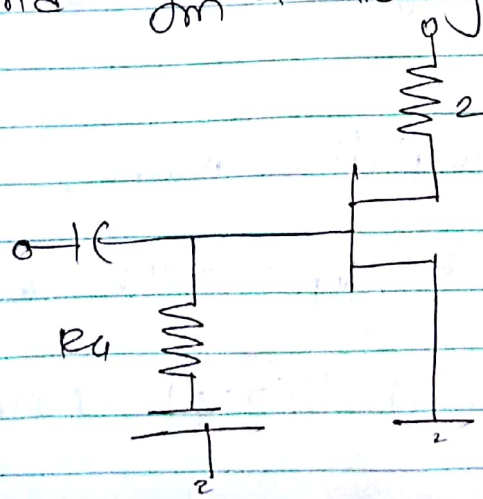
Q.11) Design a single stage CE ampl^r to meet, $|A_v| \geq 120$, $S_{ICO} \leq 10$, $f_L = 15Hz$ $V_o = 3V$. Assume suitable V_{CC}.

Q.12) Write short note on common drain amplifier circuit & applications.

Q.13) Write short note on common gate amplifier circuit & applications.

Q.14) Draw small signal model of JFET & explain significance of each parameter.

Q.15) For the fixed bias configuration, Find g_m & voltage gain A_v.



$I_{DSS} = 10mA$

$V_p = -8V$

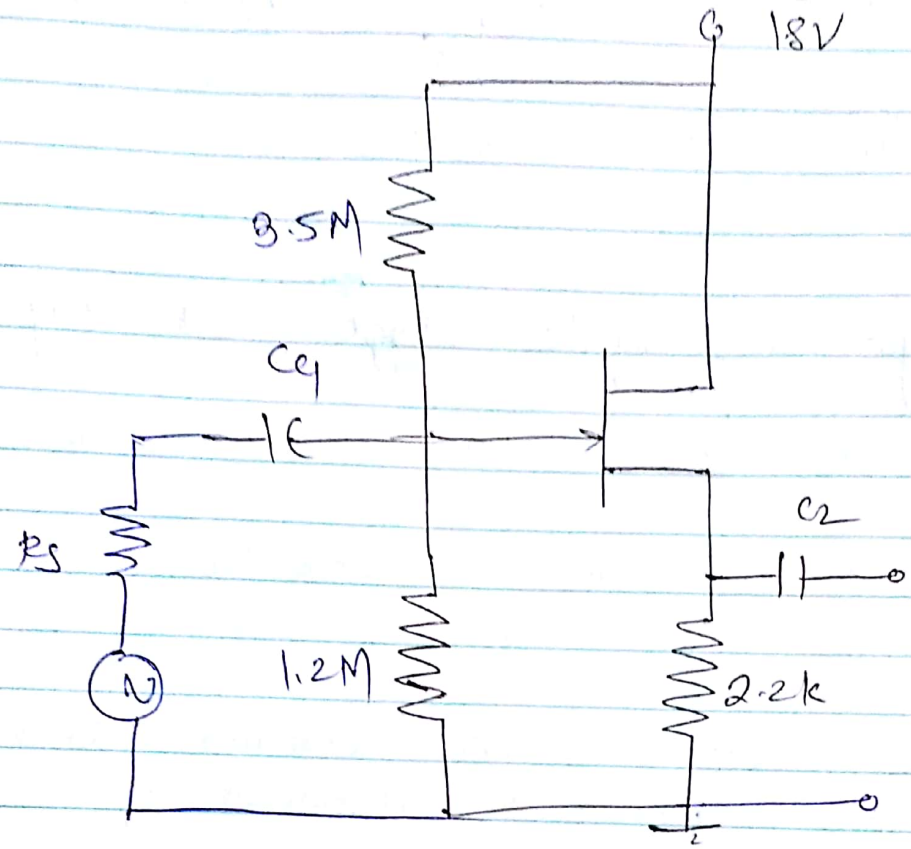
$V_{GS} = -2V$

$I_D = 5.625mA$

$Y_{OS} = 40\mu S$.

Q.16) Calculate A_v, R_i & R_o if $|V_p| = 4V$,

$I_{DSS} = 7\,mA$, $r_d = 50k$, $g_{mo} = 5000\,\mu$



Q.17) For CS Amplifier using fixed bias configuration as shown, the Q-point is, $I_{DQ} = 6\,mA$ & $V_{GSQ} = -2V$.

$I_{DSS} = 10mA$, $V_p = -7V$ respectively.

$Y_{os} = 40\mu S$.

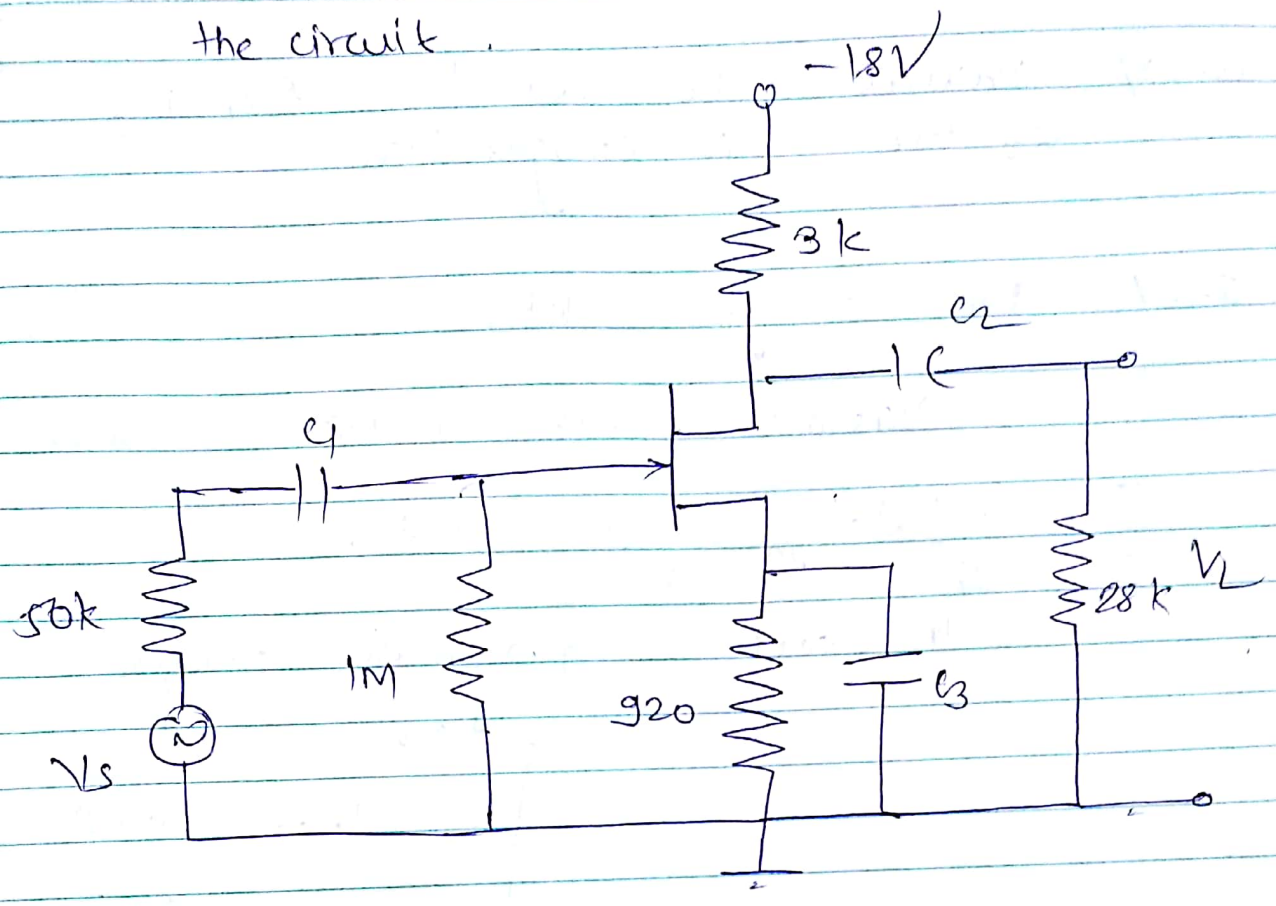
Calculate ① g_m ② r_d ③ Z_i ④ Z_o ⑤ A_v.

Q.18) For JFET amplifier shown,

$r_d = 60k$, $V_p = 3.9V$ &

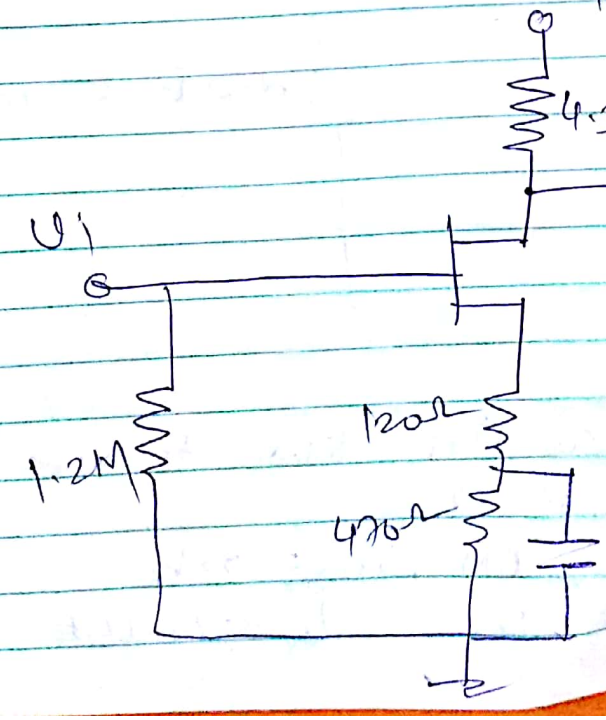
$|I_{DSS}| = 10\,mA$, If $|V_{DSQ}| = 9.2V$

Calculate the voltage gain V_L/V_s of the circuit.

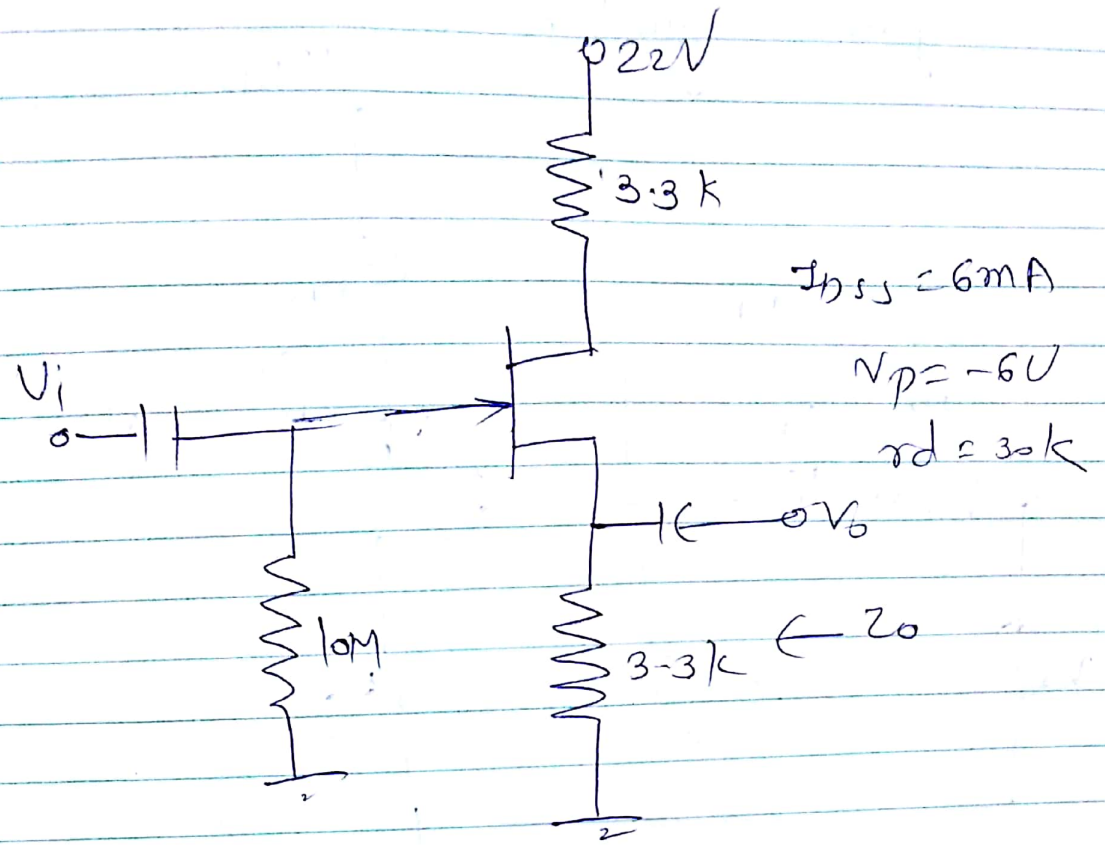


Q.17 Calculate voltage gain of given ckt.

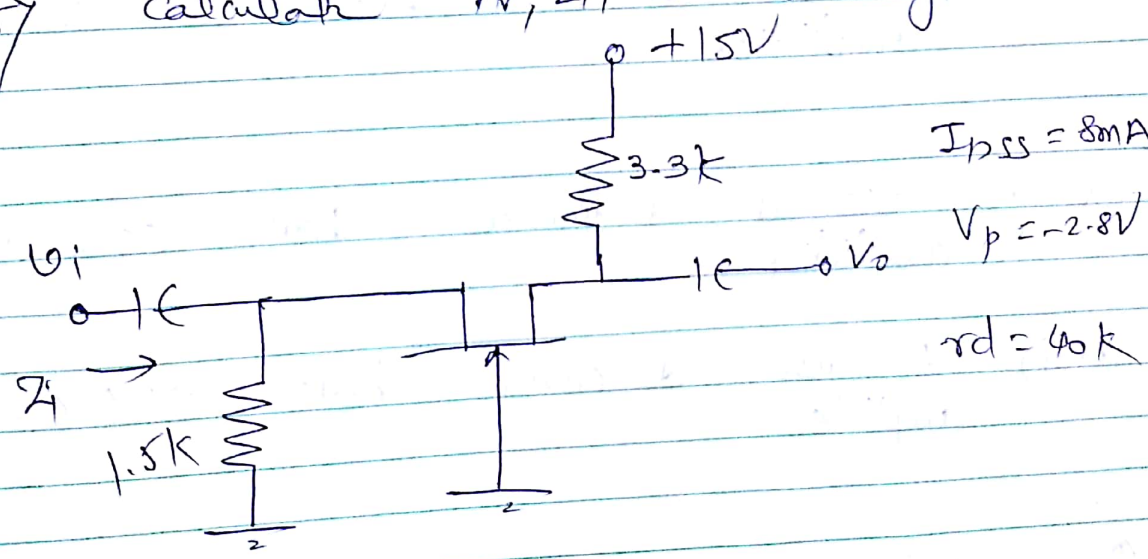
$g_m = 2.5$ ms $r_d = 50$k



Q-24) Determine Z_i, Z_o, A_V for a N/W



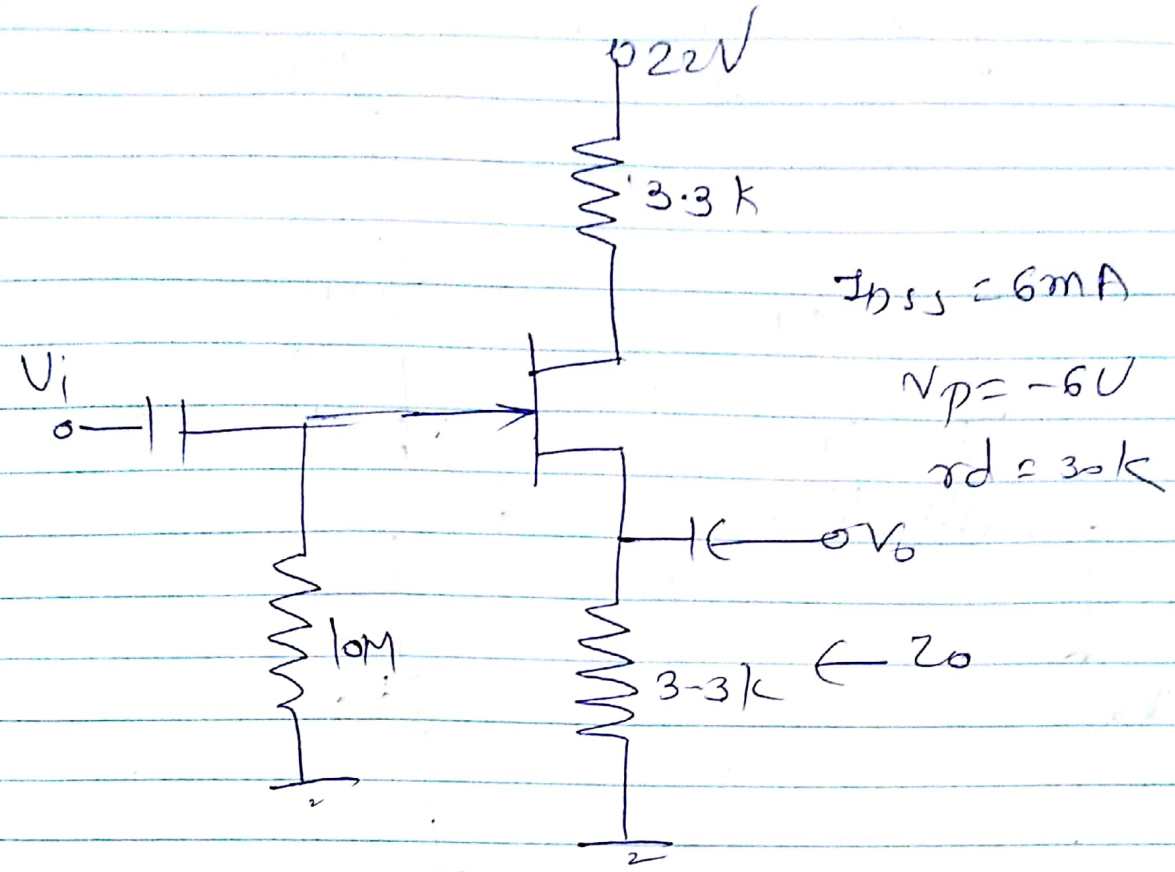
Q-25) Calculate A_V, Z_i, Z_o for a given ckt.



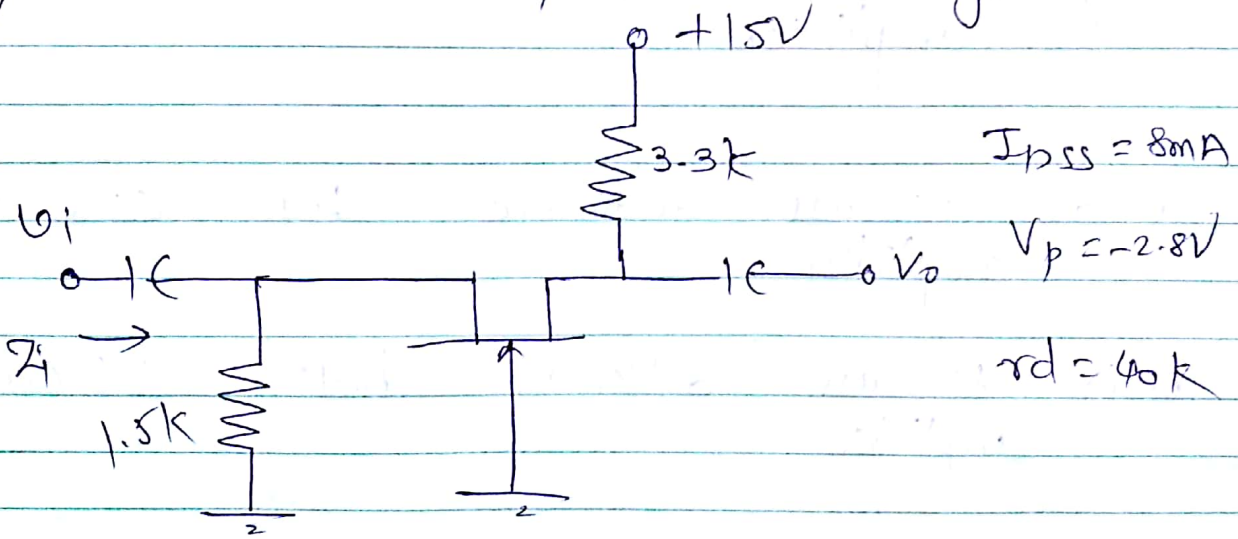
Q-26) Draw d.c equivalent ckt for voltage divider biasing with JFET amplr bypassed & Calculate A_V, Z_i & Z_o.

Q-27) Write a short note on
① g_m ② rd ③ g_{mo} ④ I_{DSS} ⑤ V_p.

Q.24) Determine Z_i, Z_o, A_V for a N/W



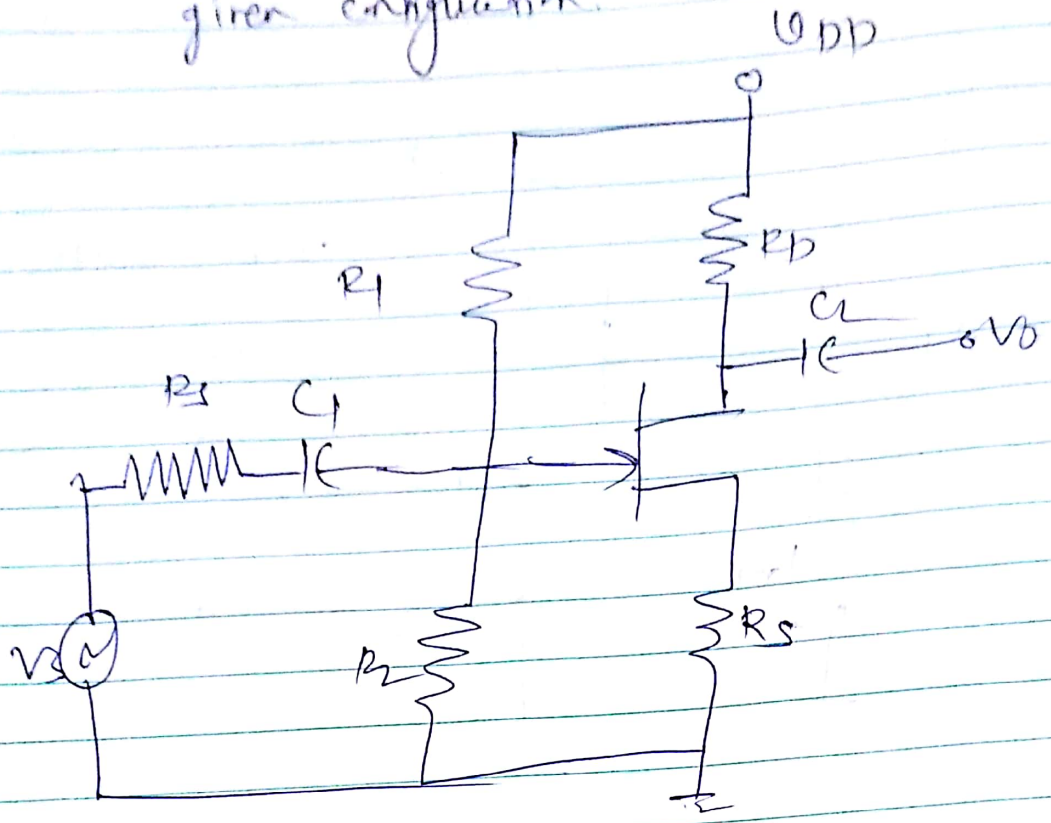
Q.25) Calculate A_V, Z_i, Z_o for a given ckt.



Q.26) Draw d.c equivalent ckt for V.D. divider biasing with JFET ampl^r bypassed R_S & Calculate A_V, Z_i & Z_o.

Q.27) Write a short note on
① g_m ② rd ③ g_{mo} ④ I_{DSS} ⑤ V_p.

Q.28) Derive the eqn for Av for the given configuration.



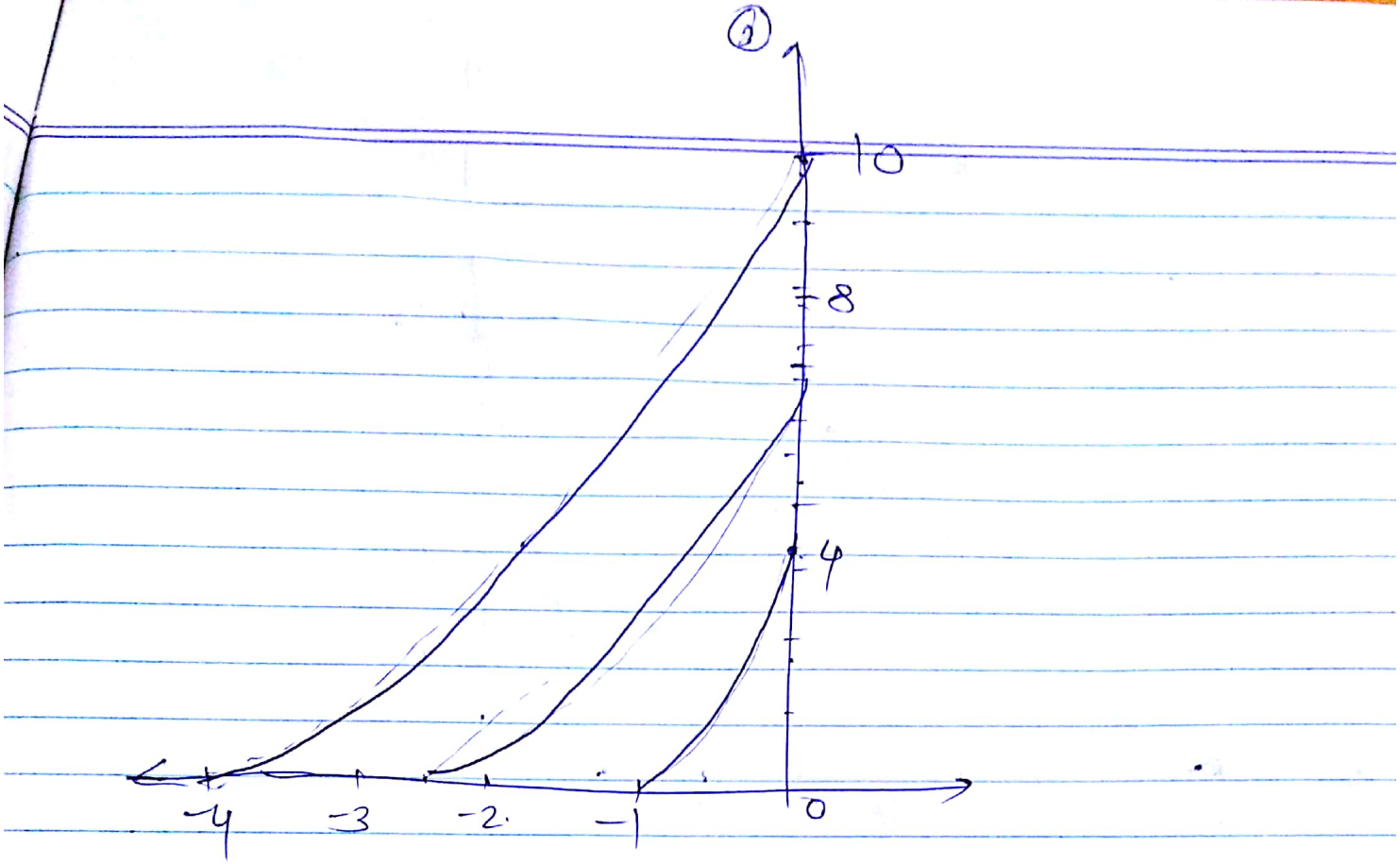
Q.29) Discuss difference betn CG & CD amplifier

Q.30) Discuss difference betn CS & CD amplifier.

Q.31) Discuss difference betn CS & CG amplifier

Q.32) Why CD configuration is called as source follower circuit? Explain.

Q.33) Design a single stage CS amplifier for $A_V = -10$, ~~$V_o = 2.5$ Vrms~~ $V_o = 2V$ at freq 20Hz. Use FET BFW-11.



(Mutual chars of BF10-11)

Q-34) In the design of CE amplifier why should R_e is large ?

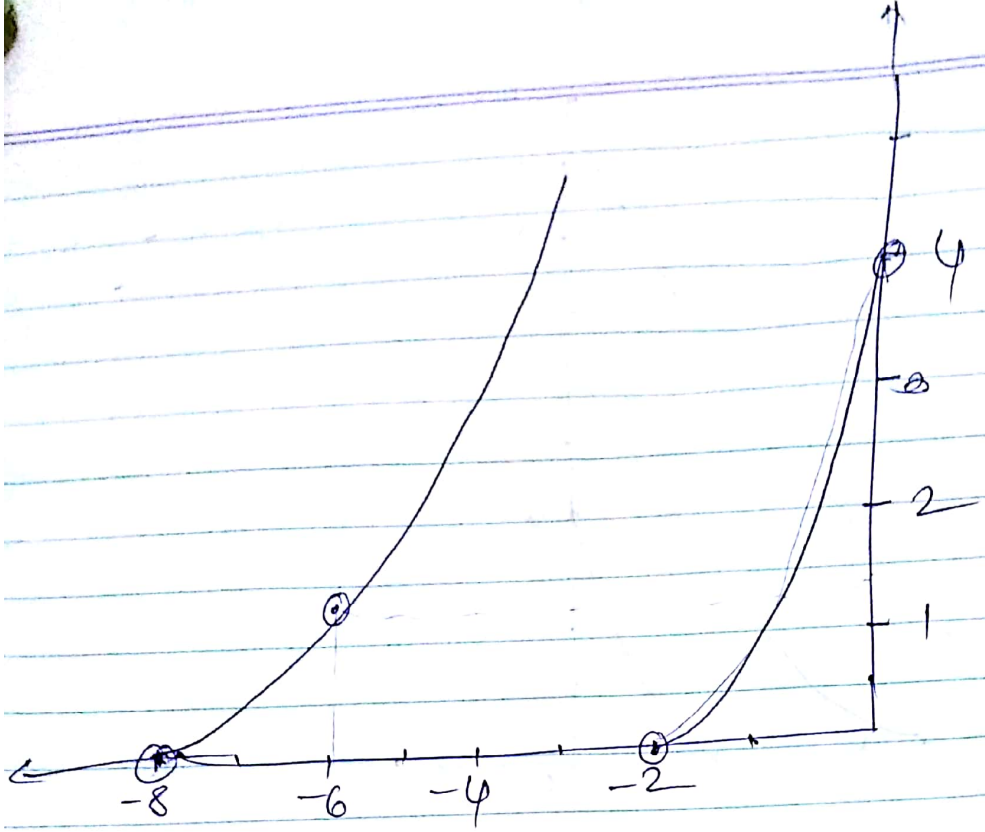
Q-35) Why R_e is always smaller than R_L in CE configuration.

Q-36) What should be the minimum value of I_E & V_E to be selected for good bias stability.

Q-37) Design single stage CS amplifier for mutual characteristics shown.

$V_{DD} = +24V$, $R_L = 120k$, $f_L = 100Hz$

Assume $g_m = 6$ mhos



Q.38) Discuss the role of coupling capacitors & bypass capacitor in Ac amplifier ckt.

Q.39) Design a single stage RC coupled CE amplifier at lower freq range 10Hz - 20kHz to give Vtg gain $A_V \geq 100$ with $S = 10$ & $V_o = 2.5V$ (rms)

Q.40) For a ckt calculate V_o & R_o.